

T-27-25

MATCHED N-CHANNEL FETS

Matched pair of symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes, mounted together in a metal S-clip.

These devices are intended for low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at $T_{amb} = 25^{\circ}\text{C}$; $I_D = 0,5 \text{ mA}$; $V_{DG} = 15 \text{ V}$

		BFS21	BFS21A
Gate cut-off current	I_G	< 0,5	0,5 nA
Gate-source voltage difference	$ \Delta V_{GS} $	< 20	10 mV
Thermal drift of gate-source voltage difference	$\left \frac{d\Delta V_{GS}}{dT} \right $	< 75	40 $\mu\text{V/K}$
Difference in transfer impedance	$\left \Delta \frac{1}{g_{fs}} \right $	< 15	7,5 Ω
Difference in penetration factor	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 1	0,5 mV/V
Common mode rejection ratio	CMRR	> 60	66 dB

MECHANICAL DATA

SOT-52 (see next page)

BFS21
BFS21A

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TOTAL DEVICE

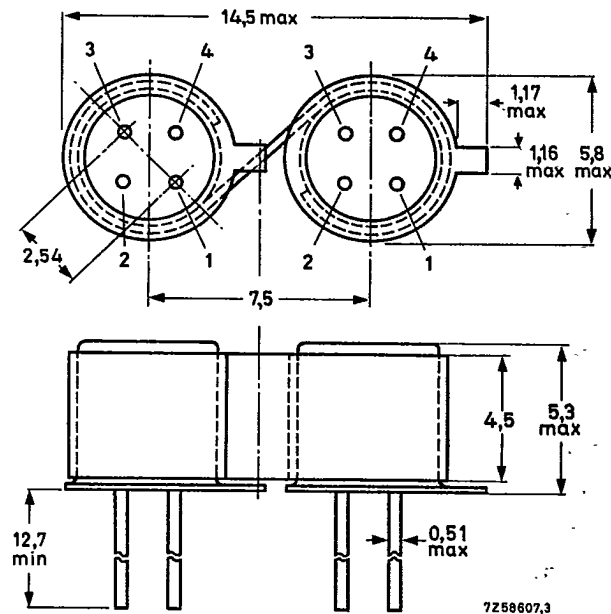
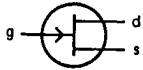
Dimensions in mm

MECHANICAL DATA

SOT52

Pinning

- 1 = source
2 = drain
3 = gate
4 = shield lead
connected
to case



Maximum lead diameter is guaranteed only for 12,7 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage between any 2 terminals	V	max.	30 V
Drain current	I_D	max.	4 mA
Gate current	I_G	max.	0,5 mA
Total power dissipation up to $T_{amb} = 100\text{ }^{\circ}\text{C}$	P_{tot}	max.	30 mW
Operating ambient temperature	T_{amb}		-20 to + 100 $^{\circ}\text{C}$

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CHARACTERISTICS (total device)

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

		BFS21	BFS21A
Drain current ratio			
$V_{DG} = 15\text{ V}; V_{GS} = 0; T_j = 25\text{ }^{\circ}\text{C}$	$\frac{I_{D1-S1S}}{I_{D2-S2S}}$	> 0.95	0.95
		< 1.05	1.05
Gate-source voltage difference			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS} $	< 20	10 mV
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS} $	< 20	10 mV
Thermal drift of gate-source voltage difference			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \frac{d\Delta V_{GS}}{dT} \right $	< 75	$40\text{ }\mu\text{V/K}$
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \frac{d\Delta V_{GS}}{dT} \right $	< 75	$40\text{ }\mu\text{V/K}$
Change of gate-source voltage difference with ambient temperature			
$T_{amb} = 25\text{ to }100\text{ }^{\circ}\text{C}$			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1}) $	< 6	3 mV
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$ \Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1}) $	< 6	3 mV
Difference of penetration factors*			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 1	$0.5 \cdot 10^{-3}$
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \Delta \frac{g_{os}}{g_{fs}} \right $	< 1	$0.5 \cdot 10^{-3}$
Difference of transfer impedances**			
$I_D = 500\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \Delta \frac{1}{g_{fs}} \right $	< 15	$7.8\text{ }\Omega$
$I_D = 100\text{ }\mu\text{A}; V_{DG} = 15\text{ V}$	$\left \Delta \frac{1}{g_{fs}} \right $	< 75	$37.5\text{ }\Omega$

- * The difference between the penetration factors is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta \frac{g_{os}}{g_{fs}} = \frac{d\Delta V_{GS}}{dV_{DG}} \text{ at } I_D = \text{constant} \right)$$

- ** The difference between the transfer impedances is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta \frac{1}{g_{fs}} = \frac{d\Delta V_{GS}}{dI_D} \text{ at } V_{DG} = \text{constant} \right)$$

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CHARACTERISTICS (continued) (total device)

Common mode rejection ratio*

$$I_D = 500 \mu A; V_{DG} = 15 V$$

$$I_D = 100 \mu A; V_{DG} = 15 V$$

		BFS21	BFS21A
CMRR	>	60	66 dB
CMRR	>	60	66 dB

INDIVIDUAL TRANSISTOR

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Drain current	I_D	max.	20 mA
Gate current	I_G	max.	10 mA
Total power dissipation up to $T_{amb} = 25^\circ$	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		-65 to + 175 °C
Junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE

From junction to ambient in free air
(for individual transistor without S-clip)

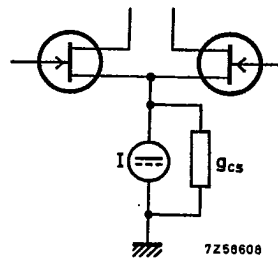
$$R_{thj-a} = 590 K/W$$

* Common mode rejection ratio

$$(CMRR)^{-1} = \Delta \frac{g_{os}}{g_{fs}} + \frac{1}{2} g_{cs} \Delta \frac{1}{g_{fs}}$$

where g_{cs} in this formula is the output
conductance of the summing current source.

The guaranteed values of CMRR apply at $g_{cs} = 0.1 \mu\Omega^{-1}$



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CHARACTERISTICS (individual transistor)

 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Gate cut-off current

 $I_D = 500\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$ $I_D = 500\text{ }\mu\text{A}; V_{DS} = 15\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$

I_G	<	0.5 nA
I_G	<	25 nA

Drain current

 $V_{DS} = 15\text{ V}; V_{GS} = 0; T_j = 25\text{ }^{\circ}\text{C}$

I_{DSS}	>	1 mA
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Gate-source cut-off voltage

 $I_D = 0.5\text{ nA}; V_{DS} = 15\text{ V}$

$-V_{(P)GS}$	<	6 V
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Transfer conductance at $f = 1\text{ kHz}$ $I_D = 500\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$

g_{fs}	>	1.0 mS
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Output conductance at $f = 1\text{ kHz}$ $I_D = 500\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$

g_{os}	<	15 μS
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Input capacitance at $f = 1\text{ MHz}$ $I_D = 500\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$

C_{is}	<	5 pF
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Feedback capacitance at $f = 1\text{ MHz}$ $I_D = 500\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$

C_{rs}	<	0.75 pF
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Equivalent noise voltage

 $f = 10\text{ Hz}$ $I_D = 500\text{ }\mu\text{A}; V_{DS} = 15\text{ V}$ $V_{DS} = 15\text{ V}; V_{GS} = 0$

$V_n\sqrt{B}$	<	200 nV $\sqrt{\text{Hz}}$
$V_n\sqrt{B}$	<	75 nV $\sqrt{\text{Hz}}$